REMARKS

The Office Action dated October 4, 2004 has been received and carefully considered. Claims 1, 2, 4-12, 14, 15, 18-21 and 26 have been amended to address various informalities and to remove "step of" phrasing. These amendments do not narrow the scope of the claims. Reconsideration of the outstanding rejections in the present application is respectfully requested in view of the following remarks.

Allowability of Claims 18-20

The Applicant notes with appreciation the indication at page 11 of the Office Action that claims 18-20 are allowed.

Anticipation Rejection of Claims 21-27

At page 2 of the Office Action, claims 21-27 were rejected under 35 U.S.C. § 102(e) as being anticipated by Morinaga (U.S. Patent No. 6,792,000). This rejection is respectfully traversed.

Claim 21, from which claims 22-27 depend, recites, in part, the limitations of a first clock recovery module having an input coupled to a first input node, and an output, wherein the first clock recovery module is to generate a clock at the output based upon received timing information transmitted in packets of a multiplexed packetized data stream before it is stored in a storage device, and a decoder having a first input coupled to the output of the first clock recovery module to receive the clock, a second input coupled the data port of the storage device to receive the select packets, and an output to provide decoded real-time data. The Examiner asserts that Figure 1 of Morinaga and the passages of Morinaga at col. 3, line 13 to col. 4, line 43, col. 4, lines 14-32, and col. 3, line 50 to col. 4, line 43 disclose these limitations. *Office Action*, p. 3. Specifically, the Examiner asserts that the limitations of the clock recovery module of claim 21 are anticipated as Morinaga allegedly discloses "time added by the receiver 22 based on the clock generated by means of the cycle timer 27 to the TS packet supplied from the PID parser 21, and supplies it to an input FIFO 23, wherein the time stamp is synchronous with the clock generated by means of the cycle timer 27." *Id.* The Examiner also asserts that Morinaga discloses the limitations of the decoder of claim 21 as Morinaga allegedly discloses an AV decoder 19, a hard disk driver 15, and the cycle timer 27. *Id.*

It is respectfully submitted that the cited passages of Morinaga do not disclose or suggest a clock recovery module to generate a clock at its output *based upon received timing information transmitted in packets of a multiplexed packetized data stream* as recited by claim 21. As disclosed by Morinaga, "the cycle timer 27 supplies the clock *having a predetermined frequency* to the receiver 22 and the transmitter 26, and the receiver 22 adds the time stamp that is synchronous with the clock generated by means of the cycle timer 27 to the TS packet supplied from the PID parser 21 and supplies it to the FIFO 23." *Morinaga*, col. 4, lines 23-28. Thus, Morinaga teaches that the cycle timer 27 has a predetermined frequency and therefore fails to disclose or suggest that the cycle timer 27 bases its clock on timing information obtained from the packetized data stream. This is collaborated by Figure 1 of Morinaga, which illustrates cycle timer 27 without any inputs by which it could receive timing information from the received transport stream output by the descrambler 13.

As Morinaga fails to disclose a clock recovery module having an output to provide a clock based upon received timing information as recited by claim 21, Morinaga necessarily fails to disclose or suggest a decoder having a first input coupled to the output of such a clock recovery module to receive such a clock as also recited by claim 21. As noted by Morinaga, the cycle timer 27 (which the Examiner incorrectly equates to the clock recovery module of claim 21) "supplies the clock having a predetermined frequency to the receiver 22 and the transmitter 26," but, as illustrated by Figure 1 of Morinaga, the AV decoder 19 does not have an input coupled to an output of the cycle timer 27. Accordingly, even if it is assumed, *arguendo*, that the cycle timer 27 were analogous to the clock recovery module of claim 21, Morinaga fails to disclose or suggest that the output of the cycle timer 27 is coupled to an input of the AV decoder 19 consistent with the limitations of claim 21.

Therefore, it is respectfully submitted that the Office Action fails to establish that Morinaga discloses or suggests each and every limitation of claim 21, as well as each and every limitation of claims 22-27 at least by virtue of their dependency from claim 21. Moreover, these claims recite additional limitations neither disclosed nor suggested by the cited references. For example, with regard to claim 26, the Examiner states that "the processing of the TS packet reproduced from the hard disk driver 15 by the AV decoder [is read] as the 'second' decoder processing, because the Av decoder 19 is adapted to process both the TS packet receiver from antenna 11 and tuner 12 and the TS packet reproduced from the hard disk driver 15." Office

Action, p. 4. However, the Applicant notes that claim 26 recites the limitations of "a second transport stream multiplexer," not a "second decoder" as inferred by the Examiner. It is respectfully submitted that the Office Action fails to establish that Morinaga discloses a second transport stream multiplexer as recited by claim 27.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 21-27 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 1-17

At page 5 of the Office Action, claims 1-13, 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Morinaga in view of Fujinami (U.S. Patent No. 5,521,922). At page 10 of the Office Action, claims 14 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Morinaga in view of Fujinami and further in view of Barton (U.S. Patent No. 6,233,389). These rejections are respectfully traversed.

Claim 1, from which claims 2-17 depend, recites, in part, the limitations of setting a system time indicator to a stored system time value, wherein the stored system time value is based on a portion of the timing data of a first portion of a packetized data stream. The Examiner relies on the cycle timer 27 and the related passages of Morinaga as allegedly disclosing these limitations. *Office Action*, p. 5-6. However, as similarly noted above, the Applicant respectfully submits that Morinaga fails to disclose or suggest that the clock output by the cycle timer 27 of Morinaga is based in any way on timing information received in the transport stream output by the descrambler 13, much less that a system time indicator of Morinaga is set to a stored system time value based on such timing information. Although the Office Action relies on Fujinami as disclosing the limitations of incrementing a system time indicator and on Barton as disclosing the limitations of a variable playback rate, the Office Action does not assert that either of Fujinami or Barton disclose or suggest the limitations of setting a system time indicator to a stored system time value, wherein the stored system time value is based on a portion of the timing data of a first portion of a packetized data stream as recited by claim 1. Accordingly, it is respectfully submitted that the Office Action fails to establish that the proposed combinations of Morinaga, Fujinami and Barton disclose or suggest each and every limitation of claim 1, as well as each and every limitation of claims 2-17 at least

by virtue of their dependency from claim 1. Moreover, these claims recite additional limitations neither disclosed nor suggested by the cited references.

In view of the foregoing, it is respectfully submitted that the obviousness rejections of claims 1-17 are improper at this time and withdrawal of these rejections therefore is respectfully requested.

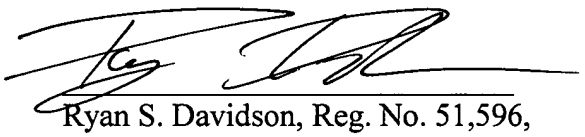
Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

22 December 2004
Date



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